

<b>Notice of References Cited</b>	Application/Control No.	Applicant(s)/Patent Under Reexamination	
	10/721,966	BUDELL ET AL.	
	Examiner Toan M. Le	Art Unit 2863	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,820,046	11-2004	Lamson et al.	703/14
	B	US-5,311,404	05-1994	Trask et al.	361/762
	C	US-6,643,831	11-2003	Chang et al.	716/4
	D	US-6,598,207	07-2003	Teague, III, Charles	716/4
	E	US-2005/0077907	04-2005	Parker et al.	324/538
	F	US-2005/0055191	03-2005	Hogyoku, Michiru	703/015
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Ruehli, Survey of Computer-Aided Electrical Analysis of Integrated Circuit Interconnections, November 1979, IBM J. Res. Develop, Vol. 23, No. 6, Pages 626-639
	V	Li et al., Substrate Modeling and Lumped Substrate Resistance Extraction for CMOS ESD/Latchup Circuit Simulation, 1999 ACM, Pages 549-554
	W	Zheng et al., Transient and Crosstalk Analysis of Interconnection Lines for Single Level Integrated Packaging Modules, 1998 IEEE, Pages 120-123
	X	Chandrasekhar et al., Modeling and Characterization of the Polymer Stud Grid Array (PSGA) Package: Electrical, Thermal and Thermo-Mechanical Qualification, 2001 Electronic Components and Technology Conference

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.